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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,473	07/11/2003	Xiaowei Deng	TI-33969	5307

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EXAMINER	
NGUYEN, VAN THU T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,473	DENG ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *19-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,23-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. Acknowledgement is made for Amendment filed on December 29, 2004.

2. Claims 1-18 are still pending.

3. Claims 23-24 are newly added.

4. Claims 19-22 are still withdrawn from further consideration.

Response to Arguments

5. Applicant's arguments filed December 29, 2004 have been fully considered but they are not persuasive.

(a) For Eto reference:

Applicants' arguments have overcome 102(b) rejection of the reference.

(b) For Itoh reference:

Detail transistors connection within the NAND gate are shown in FIG. 7b. In FIG. 7b, it shows that when the N-MOS transistor having input CE is on, P-MOS and N-MOS transistors having inputs connected to output of inverter 71 are grounded, which means power down. Applicants can not base on the symbolic NAND gate itself to determine its operation. Besides, circuit 73-74 shown in FIG. 7b is identical to FIG. 3 of the invention. They should function the same.

Regarding claim 3, Applicants argue that transistors and resistors are not interchangeable. Examiner admits that. However, the Office Action did not say transistors and resistors being interchangeable, but transistors can be considered as [variable] resistors [whose resistance depend on current applied to the gate] (see Modern Dictionary of Electronics]. Besides, no where in the Specification

discloses an advantage of resistors over transistors as ague in Applicants argument, page 11.

(c) For Yanagisawa reference:

Detail transistors connection within the NOR gate are shown beneath in FIG. 16(B). In FIG. 16(B), it shows that when the P-type transistor having input a is on, P-type and N-type transistors having input b are powered down. Applicants can not base on the symbolic NOR gate itself to determine its operation. Besides, circuit shown beneath FIG. 16(B) almost identical with FIG. 1a of the invention. They should function the same as well.

Regarding claim 3, see the reply above.

(d) For Akiba reference, it is new reference.

Drawings

6. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the *driver circuitry being power down with a power switch, and that driver circuitry is between then intervention circuit and the word line as in claims 5 and 15*, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure

must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

7. The Specification is objected to because it does not describe the driver circuitry being power down with a power switch, and that driver circuitry is between then intervention circuit and the word line as in claims 5, 15.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-18, 23-24 rejected under 35 U.S.C. 102(b) as being anticipated by **Itoh** et al. (U.S. Patent No. 4,247,921)

Regarding claim 1, **Itoh** discloses, in FIG. 7b, method of reducing power consumption in a semiconductor memory device having a row of memory cells and circuitry for operating the row of memory cells, the method comprising the steps of:

providing an intervention circuit (P-MOS connecting to CE in circuit 73);

instantiating the intervention circuit within the circuitry for operating the row of memory cells, proximal to the row of memory cells;

operating the intervention circuit to retain the row of memory cells in a desired state (via CE); and

powering down, with a power switch (N-MOS connect to CE and Vss in circuit 73), the circuitry for operating the row of memory cells preceding the intervention circuit (via CE and the N-MOS transistor)

(See column 6, line 28 to column 7 line 29).

Itoh further discloses:

Regarding claim 2, word lines are inherent within memory cell arrays 1 and 2 of FIG. 1, and the circuitry for operating the row of memory cells comprises driver circuitry, which is either P-MOS and N-MOS transistors having inputs connected to output of inverter 71, or inverter 74 itself, or both, in FIG. 7b.

Regarding claim 3, it would have been obvious to one with ordinary skill in the art to realize that transistors can be considered as resistors as well.

Regarding claim 4, the P-MOS connecting to CE in circuit 73 being a transistor as shown in FIG. 7b.

Regarding claim 5, inverter 74 is between the P-MOS connecting to CE in circuit 73 and the word line as shown in FIG. 7b.

Regarding claim 6, the P-MOS connecting to CE in circuit 73 is between the word line and the P-MOS and N-MOS transistors having inputs connected to output of inverter 71, as shown in FIG. 7b.

Regarding claims 7-8, P-MOS and N-MOS transistors having inputs connected to output of inverter 71, are grounded (power down) at the same time with the P-MOS connecting to CE in circuit 73, via signal CE, as shown in FIG. 7b.

Regarding claim 9, there's inherent nominal delay for P-MOS and N-MOS transistors having inputs connected to output of inverter 71, to be grounded after the P-MOS connecting to CE in circuit 73, to turn on.

Regarding claim 10, Itoh discloses, in FIG. 4, a method comprising providing an intervention circuit (Q'9); instantiating the intervention circuit within the circuitry for operating the row of memory cells, proximal to the row of memory cells; operating the intervention circuit to retain the row of memory cells in a desired state (via Rdi/WLi); and powering down, with a power switch (Q'6), the circuitry for operating the row of memory cells preceding the intervention circuit (via signal CE); wherein Q'9 and Q'6 are operated by two different signals RDi/Wli and CE, respectively.

Regarding claim 23, the circuitry for operating the row of memory cells preceding the intervention circuit comprising a word line pre-driver circuit 71 and 72.

Regarding claims 11-18, 24 they are rejected under U.S.C. 102(b) since they recite the same limitation as in claims 1-9, 23.

10. Claims 1-9, 11-17, 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by **Yanagisawa** et al. (U.S. Patent No. 2001/0028581) or **Akiba** et al. (P.G.Pub. 2003/0043680).

Regarding claim 1, **Yanagisawa** discloses, see transistors connection within a NAND gate shown in FIG. 16(B), a method of reducing power consumption in a semiconductor memory device having a row of memory cells and circuitry for operating the row of memory cells, the method comprising the steps of:

providing an intervention circuit (N-type transistor having input a);

instantiating the intervention circuit within the circuitry for operating the row of memory cells, proximal to the row of memory cells;

operating the intervention circuit to retain the row of memory cells in a desired state (via signal a); and

powering down, with a power switch (P-type transistor having input a) the circuitry for operating the row of memory cells preceding the intervention circuit.

Yanagisawa further discloses, see transistors connection within a NAND gate shown in FIG. 16(B):

Regarding claim 2, word lines and the NAND gate comprising a driver circuitry (P-type and N-type transistors having input b).

Regarding claim 3, it would have been obvious to one with ordinary skill in the art to realize that transistors can be considered as resistors as well.

Regarding claim 4, the N-type transistor having input a is a transistor.

Regarding claim 6, the N-type transistor having input a is between the word line and P-MOS and N-MOS having input b.

Regarding claim 7-8, the P-type transistor having input a cut off the voltage vdh supplied at the same time with the N-type transistor having input a turn on via same signal a.

Regarding claim 9, there's inherent nominal delay for P-type and N-type transistors having input b, to power down after the N-type transistor having input a turn on.

Regarding claim 23, the circuitry for operating the row of memory cells preceding the intervention circuit comprising a word line pre-driver circuit, which consists of P-type and N-type transistors having input b.

Regarding claims 11-14, 16, 17, 24, they are rejected under U.S.C. 102(e) since they recite the same limitation as in claims 1-4, 6-9, 23.

Regarding claim 1, **Akiba** discloses, in FIG. 13, a method of reducing power consumption in a semiconductor memory device having a row of memory cells and circuitry (one of 65s) for operating the row of memory cells, the method comprising the steps of:

providing an intervention circuit (N-type transistor 69);

instantiating the intervention circuit within the circuitry for operating the row of memory cells, proximal to the row of memory cells;

operating the intervention circuit to retain the row of memory cells in a desired state (via signal PD); and

powering down, with a power switch (P-type transistor 66) the circuitry for operating the row of memory cells preceding the intervention circuit (via Power Down signal PD)

(See paragraphs [0086]-[0089])

Akiba further discloses, as shown in FIG. 13:

Regarding claim 2, word lines and the circuitry comprising driver circuit, consisting either transistors 66, 67, 68 or transistors 70, 71, or all (see paragraphs [0061]-[0063]).

Regarding claim 3, it would have been obvious to one with ordinary skill in the art to realize that transistors can be considered as resistors as well.

Regarding claim 4, transistor 69 is a transistor.

Regarding claim 5, transistors 70 and 71 is between the transistor 69 and word line.

Regarding claim 6, transistor 69 is between transistors 66-68 and the word line.

Regarding claim 7-8, transistor 66 turns off voltage VDD supplied to transistors 67-68 at time as transistor 69 turn on via signal PD.

Regarding claim 9, there's inherent nominal delay for transistors 67-68 to power down after the transistor 69 turn on.

Regarding claim 23, the circuitry for operating the row of memory cells preceding the intervention circuit comprising a word line pre-driver circuit, which consists of transistors 67-68.

Regarding claims 11-17, 24, they are rejected under U.S.C. 102(e) since they recite the same limitation as in claims 1-9, 23.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

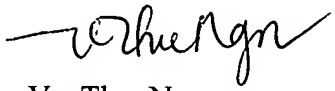
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



March 16, 2005

VanThu Nguyen
Primary Examiner
Art Unit 2824